Application

for

United States Non-Provisional Utility Patent

Title:

Through-wafer Contact to Bonding Pad

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Through-wafer Contact to Bonding Pad

Field of Invention

[0001] The invention described herein relates generally to semiconductor integrated circuit manufacturing processes. In particular, the invention relates to improved methods of making contact to the bonding pads for side or backside connection.

Background of Invention

[0002] A critical step in the manufacture of all integrated circuit devices is known as "packaging" and involves mechanical and environmental protection of the device chip as well as making electrical interconnection between locations on the silicon chip, known as bonding pads, and external electrical terminals. At present three main technologies are employed for making electrical connections to the integrated circuit: wire bonding, tape automatic bonding (TAB) and flip chip. All three technologies have deficiencies. Chip scale size packages require very small footprints to achieve space improvements. New interconnection techniques are needed to achieve even smaller footprints.

[0003] Prior art uses various means of connecting the bonding pads via external connections to the back of the chip. These external connections are typically formed in the final stages of manufacture of the integrated circuit. Additional background is found in U.S. 6,040,235 and U.S. 2003/0209772; both are incorporated herein by reference. Figure 1 shows the prior art as described in U.S. 2003/0209772.

[0004] A need exists for a more compact and less costly manufacturing techniques for making alternate contact methods to the bonding pads during IC processing.

Summary of Invention

[0005] Invention resides in the unique design of a process for making contact to the bonding pads internal to the integrated circuit die at the wafer level. Using standard IC processes, and simultaneous with other IC processes being carried out, conductive channels are formed in the silicon wafer which electrically connect the bonding pads to alternative locations on either the back of the wafer or the edge of the integrated circuit chip which will be exposed after singulation.

Brief Description of Drawings

[0006] FIG. 1 is an example of the prior art.

[0007] FIG. 2A and 2B are schematics of one embodiment of the invention.

[0008] FIG. 3A and 3B are schematics of an alternate embodiment.

[0009] FIG. 4A, 4B and 4C are schematics of an alternative embodiment.

[0010] FIG. 5A and 5B are schematics of a still alternate embodiment.

[0011] FIG. 6 are exemplary process steps for one embodiment.

Detailed Description of Embodiments

[0012] Using reactive ion etching techniques high aspect ratio features are routinely made with current IC technology. Copper metallization technology includes not only the ability to deposit seed layers but also to deposit the conductor layer and form barrier layers to prevent the diffusion of the copper into the active device regions as well as isolate it electrically from other circuit elements. All metallization schemes require a barrier material between the conductor and the device material to prevent diffusion of the conductor into the active circuit element region with subsequent degradation of circuit performance as well as maintain electrical isolation. Silicon dioxide is the most common barrier material for non-copper based metallization systems; SiO2 has the benefit of providing simultaneously electrical and material isolation. The advent of copper metallization has required extensive research to develop tantalum nitride based and other barrier systems suitable for copper.

[0013] The advent of atomic layer deposition and focused physical vapor deposition processes has allowed vertical wall features to be coated with uniform films of varying type and utility. MEM's technology teaches alternative processes for making channels in a wafer, both vertically and horizontally. Typically, these processes involve high speed reactive ion etching or wet etching techniques. Bringing these various processes together allows the current invention to be enabled.

[0014] One embodiment of the invention as sketched in Figures 2A and 2B shows a vertical channel (220) formed through the wafer (200) and either adjacent (220) or underneath (225) a bonding pad (210). This channel may be formed in one step or a

combination of steps as the integrated circuit itself is being built. In one embodiment the channel is formed prior to initial copper metallization. In this way barrier formation and seed layer formation in the channel is carried out simultaneous with copper metallization formation. The channel, having been filled with copper, then electrically connects the bonding pad on the front side (201) of the wafer to the back of the wafer (202). The size of the channel and copper cross section must be appropriate to the current carrying requirements or voltage drop requirements of the bonding pad itself. One knowledgeable in the art will understand the requirement.

[0015] An alternative embodiment is shown in FIG. 3A and 3B. In this example the conductive channel (220 or 225) extends only partially through the wafer. In this case the back surface of the wafer undergoes a polishing step to remove sufficient material (330) to expose the conductive channel. Typically, chemical-mechanical polishing is used for this process. The advantage of this embodiment is that the conductive channel may need to be only 20 to 50 microns deep; a drawback is the CMP step. A cover plate may be added to the top of the wafer for mechanical handling purposes prior to the polish step if desired.

[0016] An alternative embodiment is shown in FIG. 4A, B and C. In this example the conductive channel is formed in at least two steps, each extending only partially through the wafer. In one variation the top side channel connection (222) is formed first and the back side channel connection (442) is formed in subsequent processing. Alternatively the back side conductive channels may be formed first and then the front side. For instance, at the point in the process when the active device elements have been formed and the first

layer metallization has been covered with a passivating layer but prior to opening the vias to the first layer contacts may be a convenient point to form the backside conductive channels. In this state the wafer is well protected from most processes which may be considered for making the backside channels, giving the IC process engineer more latitude in choosing a compatible process flow. Then as the subsequent metal layers are built up on the front side of the wafer the front side conductive channel can be formed as is convenient.

[0017] Figure 5A and 5B show an alternative embodiment placing the contacts (223) at the edge of the singulated IC chip (550). In this case the conductive channel is stilled formed during the IC processing; the contact region is exposed only after chip singulation. (501) is the top or front surface of the chip and 502 is the back or bottom surface. As with all of the embodiments the conductive channel may be placed to make an edge contact, as with (523) or an under the pad contact as with (524).

[0018] One knowledgeable in the art can see that many alternative processing points can be chosen to put in a combination of front side, back side and CMP steps depending on the IC process flow and the constraints placed on the process engineer. The fundamental idea of the invention remains consistent regardless of the particular process flow.

[0019] FIG. 6 is one example of a sequence of process steps for achieving the through wafer bonding pad connections. The example process is not meant to be the exact sequence of steps used in every instance but to provide sufficient insight into the invention that one skilled in the art can reproduce the structure.

[0020] Alternative uses for these conductive channels can be envisioned. For example, copper is a better thermal conductor than silicon. A copper channel, or channels, may be placed in close proximity to a region of the IC chip which is generating an excessive amount of heat. In this way the heat is "piped" to the backside of the die and removed by contact with the packaging material. Frequently die are mounted on diamond interposers placed between the chip and the package material to facilitate heat conduction away from the die. One embodiment is that the heat sinking channels are thermally connected to a diamond interposer to improve heat removal from the IC. Alternative ways of performing this task are obvious to those skilled in the art. All of the alternatives will rely on a thermally conductive channel comprised of material with a thermal conductivity higher than silicon and, as required, with a suitable barrier material between the conductive material and the silicon.

[0021] It is apparent that in a wafer of this construction the term "bonding pad" is used for historical purposes only. Maintaining a region on the chip which can be used as a wire bonding pad or bump attachment location is a convenience that may not be necessary. In an alternative embodiment the "bonding pad" becomes a location for the conductive channel to electrically connect to the desired circuit elements without the necessity of being a functional wire bonding pad. Of course this embodiment requires an alternative scheme for electrical testing, also known as "wafer sorting", at the wafer level. One alternative would be to make contact through the conductive channels on the back of the wafer, as opposed to using the wire bond pads on the front.

[0022] In using this concept certain design rules must be established for through hole sizes, isolation material and separation distances from active components. These rules are a function of the minimum feature size of the integrated circuit and overall process capability of the particular manufacturing facility.

[0023] Foregoing described embodiments of the invention are provided as illustrations and descriptions. They are not intended to limit the invention to precise form described. In particular, it is contemplated that functional implementation of invention described herein may be implemented equivalently in hardware, software, firmware, and/or other available functional components or building blocks. Other variations and embodiments are possible in light of above teachings, and it is thus intended that the scope of invention not be limited by this Detailed Description, but rather by Claims following.